REMARKS

This is in full and timely response to the Final Office Action mailed on November 7, 2002, Reexamination in light of the following remarks is respectfully requested.

Claims 13-37 are pending in this application, with claims 13, 18, 22, 26, 30 and 34 being independent. No new matter has been added.

This amendment *prima facie* places the case in condition for allowance. Alternatively, it places this case in better condition for appeal. Accordingly, entry of this amendment is respectfully requested.

Applicant, seeking review of the *prematureness* of the final rejection within the Final Office action, respectfully requests reconsideration of the finality of the Office action for the reasons set forth hereinbelow. See M.P.E.P §706.07(c).

Claim objections

In response to the claim objections made within the Final Office Action, the claims have been amended as requested by the Examiner.

Rejections under 35 U.S.C. §103

Claims 13-25 were rejected under 35 U.S.C. §103 as allegedly being obvious over U.S. Patent No. 5,850,187 issued to Carrender et al. (Carrender) in view of U.S. Patent No. 5,418,353 issued to Katayama et al. (Katayama) and of U.S. Patent No. 5,010,237 issued to Kawana.

This rejection is respectfully traversed, at least for the following reasons.

Within claims 13-25, the clock generation circuit uses a received signal to generate a clock signal and a sampling signal. The sampling signal has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels is generated during each cycle of the clock signal, and a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses. These features are depicted at least within figures 1 and 5 of the specification as originally filed. Nevertheless, these features are not found within Carrender, Katayama and Kawana, either individually or as a whole.

Specifically, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, as claimed. For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose, teach or suggest the generation of a clock signal, and also fails to disclose, teach or suggest the generation of a sampling signal. Figure 2 of Carrender arguably teaches the existence of controller 210 that supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received signal to generate the clock signal. Figure 5 of Carrender arguably teaches the presence of received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

The Final Office Action contends that column 4, lines 10-43 of Carrender teaches the existence of a plurality of pulses formed during each cycle of the clock signal. But as noted hereinabove, the generation of a clock signal as claimed is not found within Carrender. Instead, the passage cited within the Final Office Action merely teaches first and second plurality of signal cycles (column 4, lines 18-20).

Further note that figures 13, 15, 16, 20, 22 and 24 of Katayama fail to disclose, teach or suggest a plurality of logic levels generated during each cycle of the clock signal, wherein a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses, as claimed.

While Kawana arguably teaches an IC card system, Kawana fails to disclose, teach or suggest the above-noted features deficient within Carrender and Katayama. For example, the use of a received signal to generate a clock signal and a sampling signal or a plurality of logic levels generated during each cycle of the clock signal are not found within Kawana. Withdrawal of this rejection and allowance of the claims is respectfully requested.

Claims 26-37 were rejected under 35 U.S.C. §103 as allegedly being obvious over Carrender in view of U.S. Patent No. 5,574,754 issued to Kurihara et al. (Kurihara).

This rejection is respectfully traversed, at least for the following reasons.

Within claims 26-37, a received signal is used to generate a clock signal. In addition, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with said received signal. These features are explained at least within figures 6 and 10 of the specification as originally filed. Yet, these features are not found within Carrender and Kurihara, either individually or as a whole.

In particular, failings in the teaching of Carrender have been noted hereinabove. In particular, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, as claimed. For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose, teach or suggest the generation of a clock signal, and also fails to disclose, teach or suggest the generation of a sampling signal. Figure 2 of Carrender arguably teaches the existence of controller 210 that

supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received signal to generate the clock signal. Figure 5 of Carrender arguably teaches the presence of received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

While Kurihara arguably teaches a sliding correlator, Kurihara fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal. Instead, figure 2 depicts input signal as a delayed input signal OUTPUT 1 and further depicts input signal as an non-delayed input signal OUTPUT 2 that are multiplied by multipliers 12, 13 and compared by comparator 16, but fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal, as claimed.

Figure 4 of Kurihara arguably depicts input signal as a digitized input signal from correlating unit 27 and further depicts a digitized input signal from correlating unit 28 (column 7, lines 48-49). While figure 4 depict clock generator 32, figure 4 fails to disclose, teach or suggest the use of a received

signal to generate a clock signal, as claimed. Withdrawal of this rejection and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number.

Respectfully submitted,

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APPENDIX

IN THE CLAIMS

Please amend the claims as follows.

13. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

14. (amended) The ~~. A~~ portable electronic apparatus according to claim 13, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

15. (amended) The ~~. A~~ portable electronic apparatus according to claim 13, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

16. (amended) The ~~. A~~ portable electronic apparatus according to claim 13, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

17. (amended) The ~~. A~~ portable electronic apparatus according to claim 16, wherein said received signal is a modulated signal.

18. An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said IC card by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate received data.

19. (amended) The ~~. An~~ IC card according to claim 18, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

20. (amended) The ~~An~~ IC card according to claim 18, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

21. (amended) The ~~An~~ IC card according to claim 18, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

22. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said reader/writer by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

23. (amended) The ~~. A~~ reader/writer according to claim 22, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

24. (amended) The ~~. A~~ reader/writer according to claim 22, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

25. (amended) The ~~. A~~ reader/writer according to claim 22, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

26. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

27. (amended) The ~~. A~~ portable electronic apparatus according to claim 26, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

28. (amended) The ~~A~~ portable electronic apparatus according to claim 26, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

29. (amended) The ~~A~~ portable electronic apparatus according to claim 26, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

30. An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said IC card by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said

received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

31. (amended) The ~~. An~~ IC card according to claim 30, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

32. (amended) The ~~. An~~ IC card according to claim 30, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

33. An IC card according to claim 30, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

34. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said reader/writer by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

35. ~~A~~. (amended) The reader/writer according to claim 34, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

36. ~~A~~. (amended) The reader/writer according to claim 34, wherein said first direction is an increasing direction and said

direction opposite to said first direction is a decreasing direction.

37. ~~A~~. (amended) The reader/writer according to claim 34, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

ABSTRACT OF THE DISCLOSURE

A portable electronic apparatus comprises a detecting element for detecting a high-frequency signal received by an antenna and for outputting the detected signal, a sampling element for sampling the detected signal with regard to a frequency higher than a clock frequency of the detected signal and for outputting sampled results, and a decoding element for decoding data transmitted by the high-frequency signal by use of the signal level distribution of the detected signal derived from the sampled results.